layers tolerate multiple switching cycles without significant loss in the absorbance of their colored state.

Our results demonstrate that ultrathin platinum films are viable substrates for the preparation and characterization of electrochromic monolayers. They withstand the stress associated with conventional voltammetric techniques and are sufficiently robust to tolerate the electrochemical analysis of chemisorbed monolayers over a wide potential window. Furthermore, their high transmittance in the visible region permits the spectroscopic interrogation of a single layer of chemisorbed chromophores in transmission mode. Under these conditions, the absorbance of an electroactive and chromogenic self-assembled monolayer can be switched reversibly by addressing the platinum substrate with appropriate voltage stimulations. This protocol for the electrochemical switching of chromogenic monolayers can be easily extended from ruthenium-containing thioethers and bipyridinium thiols to a broad spectrum of electrochromic building blocks. Therefore, our findings can facilitate the preparation and characterization of a diverse range of functional nanostructured materials.

Experimental

The transparent platinum electrodes (surface roughness= 6 %) were prepared according to a literature procedure [7] and then optimized for the spectroelectrochemical measurements [10]. Water (resistivity = 18.2 MΩ cm) was purified with a Barnstead International NANOpure Diamond Analytical system. Compounds **1** and **4** were synthesized following protocols reported in the literature [7a,9d]. The synthesis of **3** is illustrated in Figure S1 of the Supporting Information. All other chemicals and materials employed were purchased from commercial sources and used as received. All measurements were performed in aqueous KCl (0.1 M) using a CH Instruments 660 electrochemical workstation in conjunction with a Varian Cary 100 Bio spectrometer. The model compounds **1** and **2** were analyzed with a CH Instruments 140 spectroelectrochemical cell (path length = 1.54 mm) incorporating an indium tin oxide working electrode, a platinum counter electrode, and a platinum pseudoreference electrode. The monolayers were prepared by maintaining the transparent platinum substrates in either methanol solutions of **3** (0.1 mM) for 24 h or methanol/chloroform (1:2) solutions of **4** (0.3 mM) for 1 h. After rinsing with methanol, the modified electrodes were integrated in a custom-built spectroelectrochemical cell, together with a platinum wire counter electrode and a Ag/AgCl reference electrode. The cell was mounted in the sample compartment of the spectrometer and the absorbance of the monolayers at 600 nm was monitored in transmission mode.

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[8] Multiple and consecutive cycles within the potential windows of Figures 2a,c had negligible influence on the redox waves. Thus, both films were stable under these experimental conditions.

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ZnO Nanorod Logic Circuits**

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Metal oxide nanostructures[1–4] are potentially ideal functional components for nanometer-scale electrical,[5,6] optical,[7] magnetic,[8] and superconducting device applications, thanks to the wide variety of crystal structures and metal ions that constitute the oxides, along with their great natural abundance and excellent environmental compatibility. In particular, metal oxide semiconductors exhibit an air-stable surface without the formation of an insulating native oxide layer,

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which can realize clean and abrupt metal/semiconductor (M/SC) interfaces without any specific oxide-etching process. Nevertheless, nanodevice applications using metal oxide nanostructures have rarely been reported.[9,10] Their applications on a real electronic circuit level have been limited even for metal oxide bulk materials.[11] This results from a lack of high-quality epitaxial or single-crystalline films and difficulty in controlling metal/oxide junction characteristics. However, single-crystalline oxide nanostructures may solve these problems as they have already facilitated the fabrication of high-quality ZnO nanorod metal-oxide semiconductor field-effect transistors (MOSFETs) exhibiting field-effect electron mobilities as high as 1000 $cm^2\,V^{-1}\,s^{-1}$.[12] Pt Schottky diodes based on ZnO nanowires were also demonstrated by Heo et al. to show an ON/OFF current ratio of ~6 at 0.15/–5 V bias.[13] Meanwhile, further control of the metal/oxide junction characteristics to either good ohmic or Schottky contacts on oxide nanomaterials would readily enable creation of many other oxide-based electronic nanodevices. Here, the fabrication of high-performance metal oxide nanodevices, including high-performance metal semiconductor field-effect transistors (MESFETs) and logic gate devices, is reported.

Single-crystal ZnO nanorods, i.e., transparent conducting oxide (TCO) nanocrystals with high mobility and a low defect concentration, were used for the fabrication of high-performance field-effect transistors including both MOSFETs and MESFETs. ZnO nanorods with diameters of 20–100 nm were prepared using catalyst-free metal–organic vapor-phase epitaxy (MOVPE).[14] For ZnO nanorod device fabrications, low-resistance ohmic contacts on ZnO nanorod ends were then made using electron-beam lithography and metal evaporation of Au/Ti layers.[12] In particular, Schottky diodes (Fig. 1a) were fabricated using Schottky barrier rectifying contacts formed between a ZnO nanorod and a Au metal electrode. Furthermore, these M/SC Schottky contacts can be used as a local gate for the development of high-gain MESFETs (Fig. 2). These active devices can be integrated into sophisticated diode circuits for OR and AND logic operations (Figs. 3a,b) or into transistor circuits such as NOR and NOT logic gates due to their high voltage and signal-power gains (Figs. 3c,d).

Figure 1b shows a typical current versus voltage (I–V) characteristic curve of ZnO nanorod Schottky diodes. The Au/ZnO contacts in the diodes resulted in nonlinear and asymmetric behavior in the I–V curve with a turn-on voltage of 0.5 V for the forward bias. No significant reverse-bias breakdown was observed for reverse voltages up to –5 V. In particular, a forward-to-reverse bias current ratio (I_f/I_r) was as high as 10^5–10^6, comparable to that of bulk or planar M/SC Schottky diodes (Au/ZnO single crystals:[15] $I_f/I_r = \sim 10^3$–10^7, Ag/ZnO epilayers:[16] $I_f/I_r = \sim 10^5$–10^7), indicating excellent electrical characteristics of ZnO nanorod Schottky diodes.

I–V characteristic curves of ZnO nanorod Schottky diodes at forward bias are analyzed in terms of thermionic-emission theory.[17] From the slope of the straight line in an ln(I) versus V plot (typically for $0.1 \leq V \leq 0.4$ V), the ideality factor (η) was

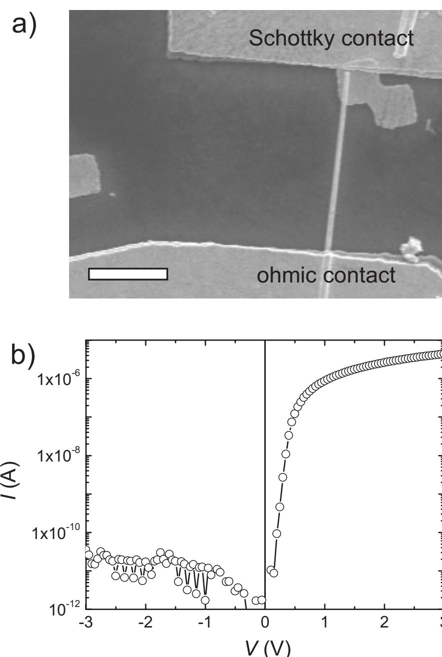

Figure 1. ZnO nanorod Schottky diode. a) Scanning electron microscopy (SEM) image of a ZnO nanorod-based Schottky diode. Scale bar, 2 μm. b) Typical I–V characteristic curve for ZnO nanorod Schottky diodes.

extracted to be 1.2, similar to that for bulk ZnO Schottky diodes ($\eta = 1.03$–1.86).[15,16,18] In general, surface state and sharp edge effects in M/SC junctions increase when scaling down the device size,[19,20] which results in a large deviation of η from unity (for example, $\eta = 7$–9 for Au nanocontacts on ZnO nanorods,[21] $\eta = 18$ for Al/GaN nanowire Schottky diodes,[22] and $\eta = 5$ for Au nanocontacts on Si[20]). Meanwhile, the observation of the I–V characteristic curve with the ideality factor value close to unity for the ZnO nanorod Schottky diodes presumably results from both high-quality ZnO nanorods and the well-defined interface between ZnO nanorods and Au metal pads.

MESFETs were also fabricated by employing an M/SC Schottky junction as a local gate. As shown in Figure 2a, Au/Ti was used for a source–drain (S–D) ohmic contact at the ends of a ZnO nanorod, while Au was used for the gate material. Figure 2b shows typical I–V characteristic curves of ZnO nanorod MESFETs depending on the measurement geometry. The I–V curve measured between the source–drain shows a straight line, indicating a good ohmic contact between the ZnO and Ti metal layers. In contrast, I–V curves measured between gates and sources or drains exhibited excellent rectifying behavior with a turn-on voltage of 0.5 V, similar to that of the ZnO Schottky diode in Figure 1b.

Figure 2c shows typical I_{sd}–V_{sd} characteristic curves of the ZnO nanorod MESFETs as a function of local Schottky gate bias (V_{lg}). Conductance shows a drastic decrease with increasing applied negative V_{lg} and, even at a low reverse voltage of –2 V, this transistor is fully turned off because, as expected for

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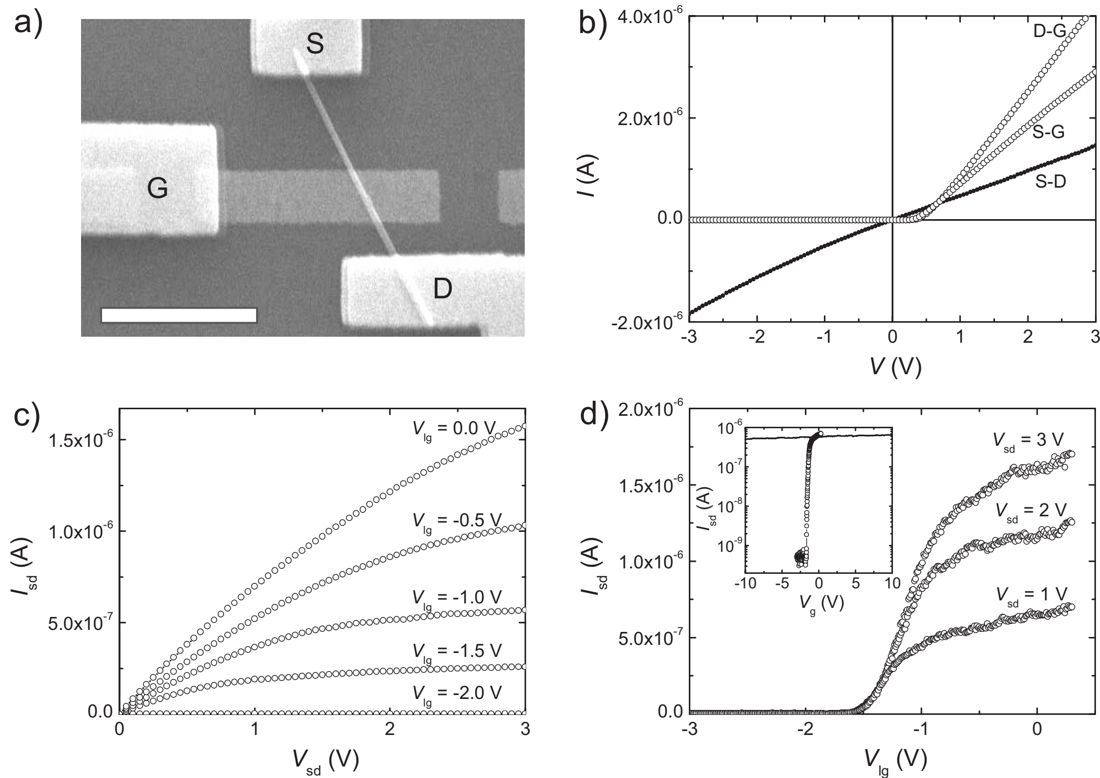

Figure 2. ZnO nanorod MESFET. a) SEM image of ZnO nanorod MESFET using Au as a Schottky gate electrode material. S: source; G: gate; D: drain. Scale bar, 2 μm. b) Typical *I–V* characteristic curves depending on measurement geometry. Source–drain (S–D) measurements show a linear and symmetric *I–V* curve, resulting from ohmic contact formation between ZnO and Ti metal layers. For both source–gate (S–G) and drain–gate (D–G) measurements, rectifying *I–V* curves are observed. c) I_{sd}–V_{sd} characteristic curves of ZnO nanorod MESFET as a function of V_{lg}. d) I_{sd}–V_{lg} characteristic curves. (Inset) log scale plots of I_{sd}–V_g curves for V_{lg} (open circles) and V_{gg} (solid line) under $V_{sd} = 1.0$ V.

n-channel MESFETs, reverse bias V_{lg} induces a space charge region under the metal gate which modulates channel conductance.[17]

Additional I_{sd}–V_{lg} curves under different V_{sd} were investigated to determine the key characteristics of FETs (Fig. 2d). The transconductance (g_m) that is obtained from the linear portion of the curve has a maximum value of 2 μS. Assuming that an effective channel width (W) equals the nanorod diameter of 100 nm, we get normalized transconductance (g_m/W) of 20 μS μm^{-1}, one order of magnitude larger than that of the ZnO nanorod MOSFETs (1.4 μS μm^{-1}),[12] and comparable to those of state-of-the-art MESFETs based on high-quality GaAs (36 μS μm^{-1})[23] and GaN (23–70 μS μm^{-1})[24,25] epitaxial films. Furthermore, the subthreshold swing (S), another key characteristic FET parameter, is as low as 100–200 mV decade^{-1} (inset in Fig. 2d) for V_{lg}, which is comparable to conventional MESFETs based on GaAs epilayers,[26] whereas an extremely weak conductance response to gate bias within an order of magnitude change is observed for global silicon back gates (V_{gg}).

This unique device layout, which utilizes M/SC Schottky barrier junctions, offers several advantages for digital logic circuit applications. First, in contrast to the metal/oxide/semiconductor configuration in MOSFET, MESFET has no insulating layer between a Schottky gate and a semiconductor channel, providing significant capacitive coupling. Thanks to the large capacitive coupling in the MESFET, it has both large voltage and signal power gains. This MESFET characteristic is required to drive the next device in series, which enables fabrication of high-performance logic devices, e.g., NOR and NOT gates. Moreover, the M/SC Schottky barrier junction in MESFETs modulates the channel conductance of individual semiconductor nanorods. Therefore, this kind of local gate could control transistors individually and effectively, allowing the integration of devices into more complex and functional electronic circuits.[27–29] Second, the current in Schottky barrier devices results primarily from majority carriers,[17] so that Schottky junction diodes can switch faster than *pn* junction diodes. In addition, the effective turn-on voltages of Schottky diodes are much smaller than those of *pn* junction diodes. These characteristics make the Schottky junction diode and MESFET useful in fast-switching circuit and high-frequency device applications.

High device performance, such as a large rectifying ratio in Schottky diodes and high MESFET transconductance, can be exploited to implement complementary logic. We first constructed a simple OR gate device by using a single ZnO nanorod where two Au Schottky contact electrodes were employed

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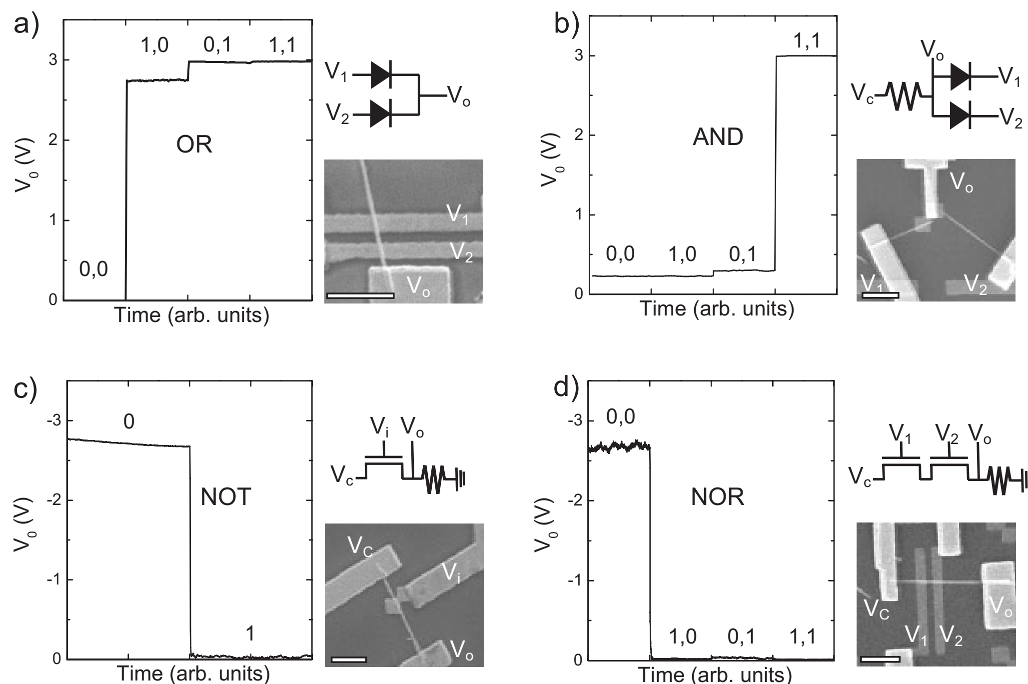

Figure 3. ZnO nanorod logic devices. a) Schematic, SEM image, and device characteristic of an OR logic gate fabricated using two Schottky diodes based on a single ZnO nanorod. The output voltage (V_o) versus the logic input configurations (V_1, V_2): (0, 0), (0, 1), (1, 0), and (1,1). Logic input 0 is 0 V and logic input 1 is 3 V. b) Schematic, SEM image, and device characteristics of an AND logic device fabricated using two ZnO nanorods. The output voltage (V_o) versus the logic inputs (V_1, V_2): (0, 0), (0, 1), (1, 0), and (1, 1), where logic input 0 and 1 are 0 and 3 V, respectively. For this measurement, the V_c of 3 V was biased and resistance (R) is 100 MΩ. c) Schematic, SEM image, and device characteristics of a NOT logic gate constructed from a ZnO nanorod. The output voltage (V_o) versus the logic inputs (V_i) of 0 and 1, where logic input 0 and 1 are 0 and –3 V, respectively. The V_c of –3 V was biased and R is 200 MΩ. d) Schematic, SEM image, and device characteristics of a NOR gate using two MESFETs fabricated on a ZnO nanorod. The output voltage (V_o) versus the logic inputs (V_1, V_2): (0, 0), (0, 1), (1, 0), and (1,1), where logic input 0 and 1 are 0 and –3 V, respectively. The V_c of –3 V was biased and R is 200 MΩ. Scale bars in a–d are 2 μm.

as V_1 and V_2 inputs, and an Au/Ti ohmic metal electrode was used as the output V_o (Fig. 3a, right). Whenever either or both of the V_1 and V_2 inputs are high (corresponding to a logic input of 1), current flows through either one of the diodes, or both, respectively. This brings the V_o output node to a high voltage (a logic output of 1). Figure 3a shows measured output voltage versus the four possible input configurations of (V_1, V_2): (0, 0), (0, 1), (1, 0), and (1, 1), where logic inputs 0 and 1 correspond to 0 and 3 V, respectively. In this device, the output is low (logic 0) only when both input voltages are low (0 V), while the other cases produce a high output voltage near 3 V (logic 1). Accordingly, this device behaves as an OR logic gate.

The SEM image of Figure 3b shows an AND gate fabricated using two adjacent ZnO nanorod Schottky diodes. In this device configuration, while two ohmic metal electrodes on ZnO nanorods are connected to V_1 and V_2 dual-inputs, the Au metal electrodes were connected to both the output and additional constant bias ($V_c = 3$ V) with a 100-MΩ resistor (Fig. 3b, right). When either one or both of the V_1 and V_2 inputs are low, current flows through the diode and the output node V_o is at a low voltage. A high output is possible only in the case of having both high inputs. The plot of output voltage versus the four possible input configurations clearly verifies an AND logic gate device function (Fig. 3b, left).

High-performance MESFETs based on single-crystal oxide nanorods can be extended to the fabrication of transistor logic gates. Figure 3c shows the basic operation of a NOT gate or inverter constructed from a single MESFET and a –200-MΩ resistor. When the input logic is 0 ($V_i = 0$ V), the nanorod channel is open and the output voltage approaches –3 V (logic 1) since the voltage drop across the transistor is relatively small and most of the voltage drops within a resistor. In contrast, with the input logic 1 ($V_i = -3$ V), the nanorod channel is fully depleted and the output voltage approaches to near 0 V (logic 0). In addition, a NOR logic gate can be made by using two transistors and a –200-MΩ resistor in series, where two parallel Au metal electrodes were configured to local Schottky gates as shown in Figure 3d. In this circuit, when both input logics are 0 (both V_1 and V_2 are 0 V), the output logic is 1, i.e., the output voltage approaches –3 V since both transistors are on and most of the voltage drops within a resistor. In the other three cases, one or both transistor channels are closed and most of the voltage drops within the transistors, producing output logic 0.

The realization of electronic circuits based on single-crystalline semiconducting oxide nanorods represents an important step toward nanoelectronics. Nevertheless, there still remain some issues to be addressed. For example, it is difficult to cas-

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cade circuits of diode logic (OR and AND logics) into multiple levels of logic gates since the voltage drop across the diodes adds up as they are cascaded in series, leading to a significant reduction in output voltage level.[30] In addition, the NOT and NOR logic circuits using extra resistors cannot be integrated easily. These problems due to the use of a diode or a resistor may be solved by hierarchical assembly and interconnection of oxide nanorod transistors.[29,31]

High-quality oxide nanorods and excellent metal/oxide semiconductor junction characteristics open up significant opportunities for the fabrication of oxide nanodevices. In particular, logic gates as well as Schottky diodes, MESFETs, and MOSFETs fabricated on ZnO demonstrate high performance in device characteristics. These sophisticated oxide electronic devices would greatly increase the versatility and power of the building blocks for the fabrication of numerous nanodevices based on metal oxides. These oxide nanorod devices may be used as components for many other multifunctional nanodevices and nanosystems by direct integration of a wide range of metal oxides such as transparent semiconductors,[6,7] piezoelectrics, ferroelectrics,[5] colossal magnetoresistors, high Curie temperature of crystallization (T_c) superconductors, and nonlinear optical materials.[32]

Experimental

Single-crystal ZnO nanorods were prepared as a starting material for ZnO nanorod devices on Al_2O_3 (001) or Si substrates using MOVPE. No metal impurity catalyst was deposited on the substrates. Details of non-catalytic ZnO nanorod growth are described elsewhere [14]. ZnO nanorods grown for 10 h with a typical mean diameter of 20–100 nm and a length of 5–10 μm were used in these studies. Using a spin-on coating technique, as-grown ZnO nanorods were dispersed on SiO_2 (250 nm)/p^+-Si substrates, where 20 nm thick Au metal patterns as both Schottky metal electrodes and alignment markers were defined. Ohmic contact electrodes and interconnect leads were defined on one side of the nanorods and metal patterns using electron-beam lithography, followed by 80 nm thick Ti and 120 nm thick Au layer evaporation and lift-off processes [12]. Meanwhile, Schottky barrier rectifying contacts were formed between ZnO nanorods and Au metal electrodes. All electrical measurements were performed in air at room temperature.

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